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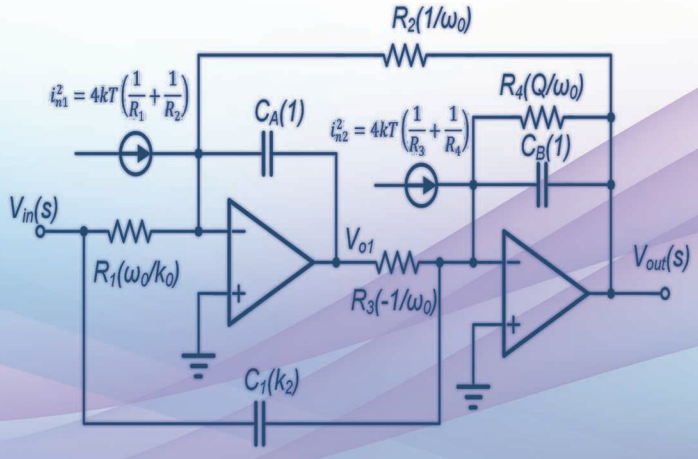

BACKGROUND: FOOTAGE FIRM, INC.

Scaling for Optimum Dynamic Range and Noise–Power Tradeoff

A review of analog circuit design techniques.

In a recent overview article [1], Prof. Yannis Tsividis reviewed the connection between dynamic range (DR), signal-to-noise ratio (SNR), the signal bandwidth, and the required power dissipation for analog circuits. As a follow-up to that tutorial, this article reviews circuit design techniques available for optimizing the DR and the tradeoff between power dissipation and SNR. The discussion is restricted to the special cases of simple active-resistor–capacitor (active-RC), active-switched-capacitor (active-SC), and transconductance-based (G_m-C) circuits. However, the principles can easily be extended to other active or passive linear circuits. Proper scaling using the proposed methods can greatly improve the figures of merit of analog and mixed-mode ICs.

Due to the many nonideal effects present in analog integrated circuits, the analog designer's task is more an art than straightforward engineering. In this article, two particular aspects of the design process are treated: the optimization of the DR and the power–SNR tradeoff. The DR (called *usable DR* in [1]) is defined as the ratio of the maximum and minimum signal powers S_{max}/S_{min}. Here, S may be a voltage, current, or charge signal. In this article, we discuss only voltage signals and noises.

It is usual to talk about the signal's "power," which in fact is the mean-square value of the signal. In an active circuit, S_{max} is usually determined by the linear ranges of the active devices (amplifiers, transconductances, etc.) in the circuit; S_{min} is usually determined by the noise in the circuit. For signal powers larger than S_{max}, one or more active blocks distort the signal; for signals smaller than S_{min}, the signal and noise become indistinguishable. At $S = S_{min}$,

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the SNR becomes 1 or 0 dB. Optimizing the DR is achieved by making the maximum value of the signal (the signal swing) close to S_{max} and reducing the noise power determining S_{min} to the lowest possible level.

The noise in the circuit may be either inherent to the physical properties of the circuit elements (intrinsic noise) or coupled into it from outside through the substrate or power lines or by imperfect ground (extrinsic noise). Inherent noises include thermal noise, caused by the random motion of charge carriers due to their thermal energy at nonzero absolute temperatures; 1/f or flicker noise, caused by charge trapping; and shot noise, caused by the granular nature of the current flow. Noise signals can be characterized by their power spectral densities (PSDs). The PSD of a noise voltage is a function of frequency f such that $PSD(f).\Delta f$ is the noise power in the frequency range f to $f+\Delta f$ for vanishing Δf.

As already mentioned, the DR is optimized by changing the amplitudes of the internal signal swings so as to make all adjustable signal powers close to S_{max}. The optimization of the power–SNR tradeoff is based on the observation that the voltage noise power in an integrated circuit can be decreased by lowering the impedance level of the circuit. For example, the PSD of thermal noise generated in a resistor R is given by $PSD_R = 4kTR$, where k is the Boltzmann constant, $k = 1.38 \times 10^{-23}$ J/K, and T is the absolute temperature [Figure 1(a)]. Reducing R reduces PSD_R. A transconductance generates an input-referred thermal noise $PSD_{Gm} = E_N.4kT/G_m$ [Figure 1(b)]. Here E_N is the excess noise factor, usually between 1 and 5, due to the additional noise contributed by the internal devices in the transconductor [1]. Increasing G_m reduces PSD_{Gm}.

Another example involves the first-order low-pass filter constructed from a noisy resistor and a capacitor (Figure 2). This structure may represent a conducting switch charging the capacitor to the input voltage. It is easy to show that the power of the voltage noise across the output terminals is $N = kT/C$. Reducing the impedance level of the whole circuit reduces R and increases G_m and C, thereby reducing all this noise. Increasing the transconductance of an MOS transistor by increasing its width can also reduce its 1/f noise.

It is obvious that external noise voltage coupling is also reduced by lowering the impedance level of the circuit, because the voltage division from the external noise source to the internal nodes of the analog circuit is enhanced.

The price paid for the reduced noise level (and, hence, for the enhanced SNR) is increased power dissipation. For fixed bias voltages, reducing the impedance level by a factor x increases all currents—and also the power dissipation—by the same factor x. The noise power reduction and the bias power enhancements are by the same factor. The optimum impedance level is thus the one that sets the noise power to the largest value tolerable by the SNR requirements and thus minimizes power dissipation.

In this article, we discuss the circuit design techniques that can achieve both DR and power–SNR optimization. First, the scaling of active-RC and active-SC stages based on operational amplifiers (op amps) is explained; then, the scaling of G_mC circuits is discussed. The final section shows some simple design examples.

Scaling Op Amp-Based Circuits

Linear active circuits are usually realized using op amps or transconductors (G_m blocks). Op amp-based circuits may operate in continuous time; in such cases, they are constructed from resistors and capacitors (active-RC circuits) or from tunable MOSFETs and capacitors (MOSFET-C circuits). Alternatively, they may operate as discrete-time circuits, in which case they use both switched and unswitched capacitors (SC circuits). All of these circuits require scaling for optimal operation.

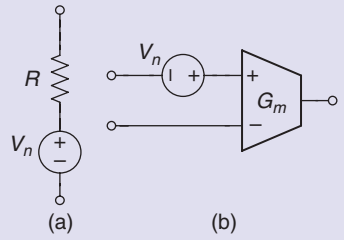

FIGURE 1: Diagrams showing noise models. (a) An equivalent model for a resistor and (b) an equivalent model for a transconductor.

Active-RC and MOSFET-C Circuits

A simple example illustrates the process of scaling active-RC circuits. Figure 3 shows a second-order active-RC filter, often called a *biquad* [2]. By choosing such frequency- and impedance-normalized element values as $R_1 = \omega_o/k_0$, $R_2 = 1/k_1$, $R_3 = 1/\omega_o$, $R_4 = -1/\omega_o$, $R_5 = Q/\omega_o$, $C_1 = k_2$, and $C_A = C_B = 1$, it realizes the transfer function

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{k_2 s^2 + k_1 s + k_0}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2}. \quad (1)$$

Here, ω_o is the pole frequency, and Q represents the pole Q. R_4 is a negative resistance, realized in the usual differential implementation by crossing leads. The initial design is obtained by matching the circuit response to the specified transfer function. This gives five nonlinear equations for the eight unknown element values. By assigning the value 1 to the feedback capacitors and choosing equal magnitudes for the input resistors R_2 and R_4 of the two integrators, the extra three degrees of freedom are absorbed, and the nonlinear equations are replaced by linear ones (see [2] for details of this process).

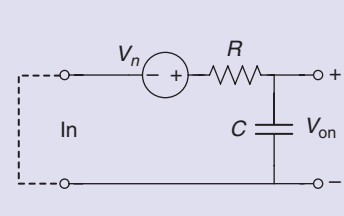

FIGURE 2: A diagram of a first-order low-pass filter. In: input current/voltage.

We can assume that the given transfer function $H(s)$ gives an optimum voltage swing for V_{out} (if not, it can be multiplied by an appropriate constant); however, the output swing of the first op amp V_{o1} is not controlled at this point.

To take care of this, drive the biquad with a full-scale sinewave input voltage, and plot the response at the output of op amp 1. The linear models of the op amps should be used for this process. Ideally, the peak swing of this response should represent the optimal choice for the amplifier. For example, let the desired swing be 1 V; if the actual swing at this point is 2 V, scaling should be used and can be performed by increasing the value of C_A to 2. If V_{out} remains the same, this reduces V_{o1} to the desired value. However, to keep V_{out} unchanged, the current into the second integrator must be restored to the original value. This is achieved by reducing the impedance of the negative resistor $R_4 = -1/\omega_o$ by the factor 2.

A straightforward generalization of the described process gives the rule for correcting an op amp's output swing. Let the ratio of the actual and desired swings be x. To restore the swing to the desired value, multiply the admittance of the op amp feedback admittance by x; to keep all other voltages unchanged, multiply also all admittances connecting the op amp output signal to the other stages by x.

This DR scaling eliminates one of the three degrees of freedom available in the design of the biquad. The other two may be used to obtain the optimum impedance levels for the two integrator stages. Consider again the first integrator. Multiplying all admittances connected to the inverting input node of the op amp by a factor y_1 leaves V_{o1} and all other voltages unchanged but changes all currents in the integrator circuit by the same factor y_1. This allows scaling the admittance of the elements R_1, R_3, and C_A to an optimal level for the SNR versus power dissipation tradeoff. The same manipulation should be performed separately with a different factor y_2 for the five elements of the second integrator.

The generalized rule for impedance-level adjustment is clearly the following. Multiply the admittances of all elements connected to the inverting input of the op amp by a smallest factor that matches the required SNR. Then, carry out the operation for every op amp separately.

A complex active-RC circuit may have several op amps. In such cases, both scaling steps must be repeated for each one. Note that impedance-level scaling does not affect the result of the DR scaling, but DR scaling changes the impedance levels. Hence, DR scaling should precede the impedance-level adjustment.

Returning to the biquad of Figure 3, the scaling steps can be summarized as follows.

1) Find the maximum voltage swing of V_{o1} at the output of op amp 1. This can be done in the frequency domain by placing a maximum amplitude sinewave V_{in} at the biquad input and sweeping its frequency in the range of interest. Compare this swing with the linear range of the op amp. Scale the impedances of all branches (feedback and feedforward) connected to the op amp output node to make the actual maximum swing close to the optimum one. (The maximum swing can also be found in the time domain by computing a histogram of V_{o1} for a large input signal V_{in}. This shows how often the various values of V_{o1} occur and what the limits of these values are.)
2) If the V_{out} swing is not optimum for op amp 2, change the constant factor of $H(s)$, or repeat step 1 for op amp 2.
3) Attach the appropriate noise source to each resistor in the first integrator. For thermal noise, use a series noise voltage source with a value $PSD_R = 4kTR$. Calculate analytically or compute the power of an equivalent input noise source V_{n1}. This source is in series with V_{in}, and it represents all noises inside the stage. Compare this noise power with the input signal power. Scale the impedance of all components of the first integrator to obtain the required SNR: reducing these impedance levels by a factor y_1 reduces the noise by $10.\log_{10}\ y_1$. Note that the process affects only the noise of the resistors. Readers should consult a textbook, such as [4], for scaling the amplifier noise.
4) Repeat step 3 for op amp 2.

The scaling of MOSFET-C circuits is similar to that of active-RC ones and does not require separate discussion.

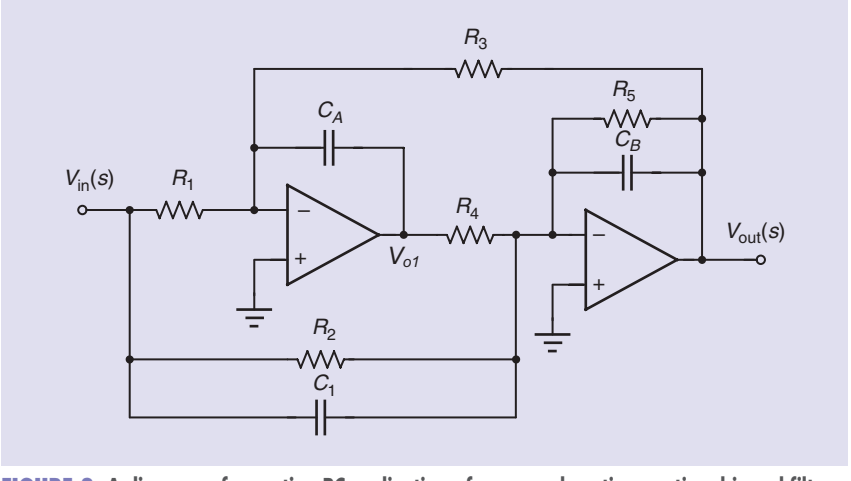

FIGURE 3: A diagram of an active-RC realization of a general continuous-time biquad filter.

Active-SC Circuits

Replacing the resistors in the active-RC biquad of Figure 3 gives the equivalent active-SC stage shown in Figure 4 [2]. Its transfer function is

$$H(z)=\frac{V_o(z)}{V_i(z)}=-\frac{(K_2+K_3)z^2+(K_1K_5-K_2-2K_3)z+K_3}{(1+K_6)z^2+(K_4K_5-K_6-2)z+1}. \quad (2)$$

As for the continuous-time biquad, both DR and SNR–power tradeoff scaling needs to be performed. DR scaling is similar to that described for continuous-time, active-RC biquads. The scaling for the optimum impedance level may also be performed similarly, if a switched capacitor branch is treated as a resistor of value $R = 1/Fc$. However, it is often done in a different way [2]. This is based on the minimum capacitance value $C_{\min}$ that can be used in the implementation. It may be specified for the technology used. $C_{\min}$ may also be determined by the required matching accuracy or the parasitic capacitances in the devices. Note that this process is distinct from the power optimization process described earlier. For the biquad of Figure 4, the process is performed in the following steps [2].

1) Compare the values of all capacitors connected or switched to the input node of op amp 1. Let the smallest in the set of these be C_i.
2) Multiply all capacitors in the set by $C_{\min}/C_i$. This does not change the values of the node voltages anywhere in the stage.
3) Repeat steps 1 and 2 for all op amps in the stage.

These operations will change the admittance level and power dissipation to the lowest value consistent with $C_i > C_{\min}$ for all i conditions, without changing the signal voltages.

Scaling G_m-C Circuits

In G_m-C circuits, the transconductances do not provide virtual grounds or buffer their output signals, which makes scaling these circuits more challenging than op amp-based ones. Figure 5 shows a G_m-C biquad [2]. In this biquad, capacitors C_A and C_B perform current integration, while the G_m blocks transform their input voltages into currents and couple the signals.

Consider the first integrator consisting of G_{m1}, G_{m4}, and C_A. For DR scaling, the value of C_A may be changed. Multiplying C_A by x, the output voltage swings of G_{m1} and G_{m4} are divided by x. This assumes that the input voltages of G_{m1} and G_{m4} remain unchanged. To achieve this, G_{m2} also needs to be multiplied by x. This keeps the output current of G_{m2} and, hence, also V_{out} unchanged.

The impedance level of the first integrator can also easily be adjusted. If the values of G_{m1}, G_{m4}, and C_A are all multiplied by the same factor y, the voltage V_{01} across C_A remains unchanged; hence, so is V_{out}. The impedance level of the integrator is, however, divided by y.

Scaling of the second integrator is made more involved by the presence of the damping transconductance G_{m3} and the feedforward capacitor C_x. Node analysis shows that the output voltage is given by

$$V_{\text{out}}=\frac{(sC_x+G_{m5})V_{\text{in}}+G_{m2}V_{o1}}{s(C_B+C_x)+G_{m3}}. \quad (3)$$

This does not allow scaling of V_{out} by a constant x without changing V_{01}. Hence, this scaling needs to be performed

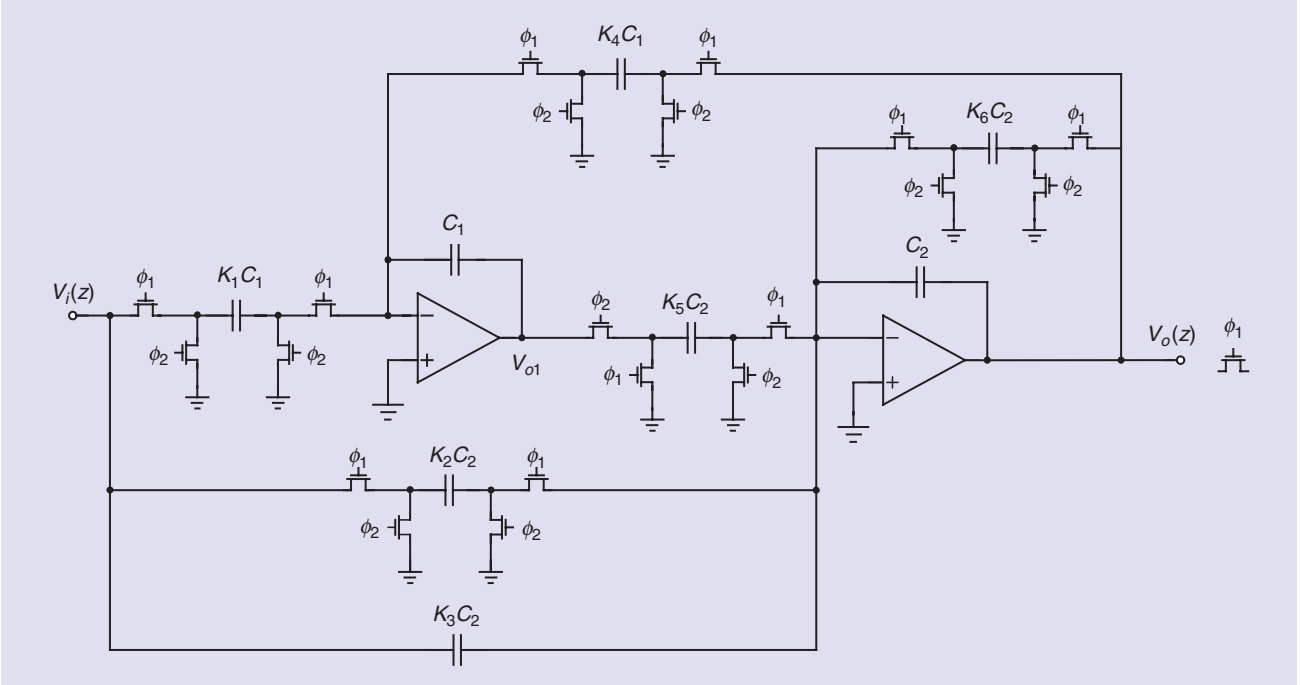

FIGURE 4: A diagram of a low-Q SC biquad filter (without switch sharing).

on the transfer function $H(s)$ before designing the circuit simply by including a constant factor to $H(s)$. If $C_x = 0$, scaling of the circuit is possible by the process described for V_{01}.

To reduce the impedance level of the second integrator by a factor y, all admittances ($sC_x, sC_B, G_{m2}, G_{m3}$, and G_{m5}) should be multiplied by y. This will not change any of the voltages, but it will increase all currents in the stage by y.

Design Examples

Figure 6 shows the implementation of a band-notch biquad with transfer function as [3]

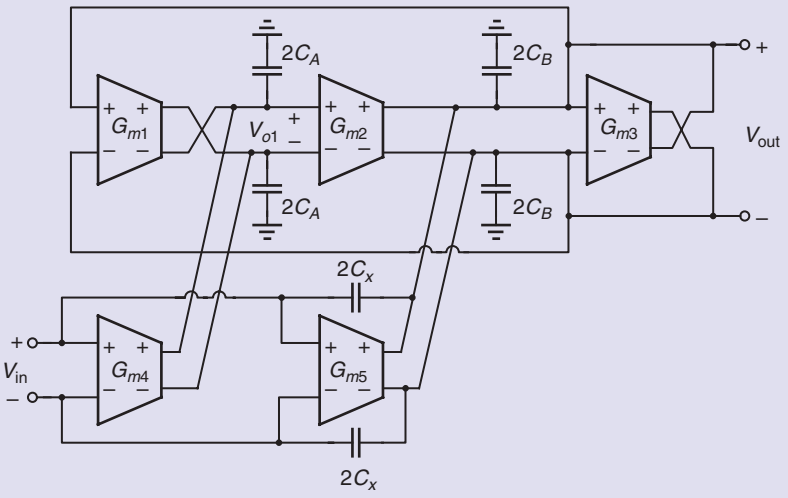

FIGURE 5: A diagram of a G_m-C biquad implementation.

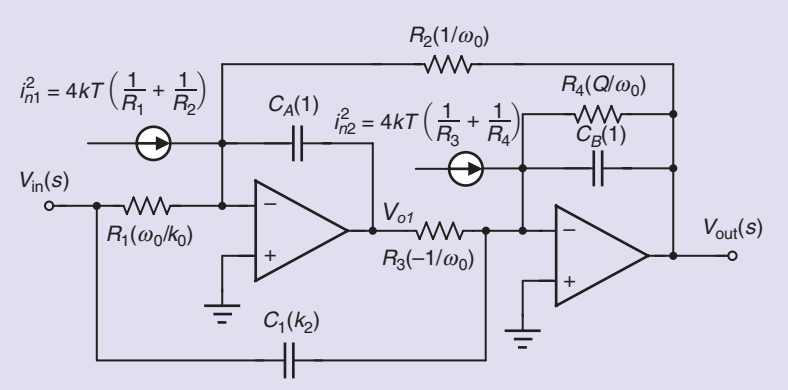

FIGURE 6: A diagram of a low-pass biquad with Q = 1.

TABLE 1. COMPONENT VALUES.

TERMS	NORMALIZED VALUES	VALUES BEFORE SCALING	VALUES AFTER SCALING
R_1	1 Ω	10 KΩ	11 KΩ (x = 1.1)
R_2	1 Ω	10 KΩ	10 KΩ
R_3	1 Ω	10 KΩ	7.937 KΩ (x = 1/1.26)
R_4	1 Ω	10 KΩ	10 KΩ
C_A	1 F	5.033 pF	6.3416 pF (x = 1.26)
C_B	1 F	5.033 pF	5.033 pF
C_1	0.1 F	0.5033 pF	0.4575 pF (x = 1/1.1)

$$H(s) = \frac{0.1s^2 + 1}{s^2 + s + 1} \tag{4}$$

and with $Q = 1$, $\omega_0 = 1$, and the notch frequency $\omega_c = \sqrt{10}$. Component values are summarized in the second column of Table 1.

If we want to map the notch frequency to 10 MHz, the notch frequency is given by [3]

$$\omega_c = \frac{1}{RC}. \tag{5}$$

Then the capacitor values can be found by

$$\frac{C}{C_N} = \frac{\sqrt{10}}{2\pi \times 10\ \text{MHz}} \times \frac{R_N}{R}, \tag{6}$$

where C_N and R_N are the normalized capacitor and resistor values, which are 1. If R = 10 KΩ, then the capacitor value becomes 5.033 pF, and the other component values can also be figured out, as shown in the third column in Table 1.

For DR scaling, the output swing of the first and second op amp before and after scaling is given in Figure 7. Here, the first op amp maximum output amplitude is 1.4, and the second is 1.1 before scaling. First, the final biquad output amplitude needs to be 1, so a scaling factor of 1/1.1 is introduced to multiply with the overall transfer function. Therefore, K_2 and K_0 corresponding to C_1 and R_1 need to be scaled. To scale the first op amp maximum swing to 1, a scaling factor of 1.1/1.4 can be used to scale C_A and R_3. The component values after scaling are given in the fourth column of Table 1.

For noise analysis, the noise current from R_1 and R_2 (Figure 6) can be modeled to the first op amp input, and then the input-referred noise voltage becomes [5]

$$v_{n1}^2 = 4kT\left(\frac{1}{R_1} + \frac{1}{R_2}\right) * R_1^2. \tag{7}$$

The noise current from R_3 and R_4 can be modeled to the second op amp input and then referred to the overall input. Its value is

$$v_{n2}^2 = 4kT\left(\frac{1}{R_3} + \frac{1}{R_4}\right) \times \left(\frac{R_4}{1 + sC_B R_4}\right)^2 \times \frac{1}{|H(s)|^2}. \tag{8}$$

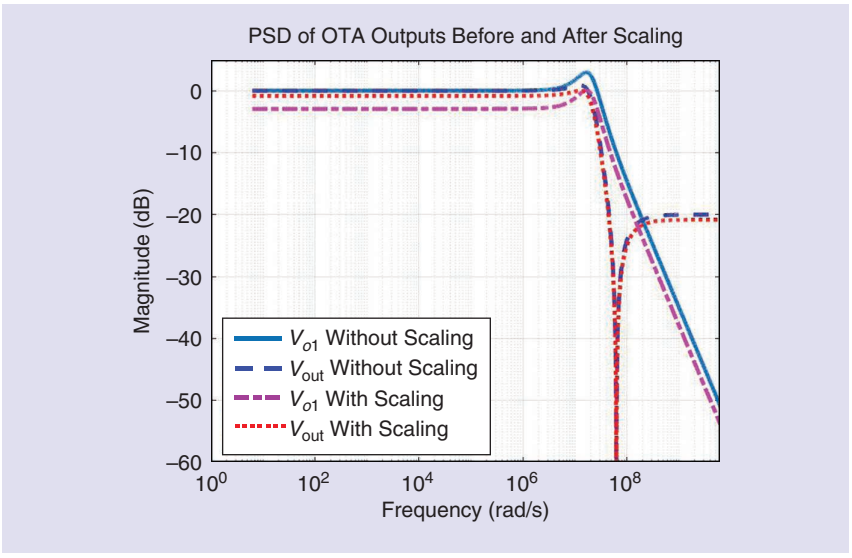

FIGURE 7: A graph showing the op amp output before and after swing scaling. OTA: operational transconductance amplifier.

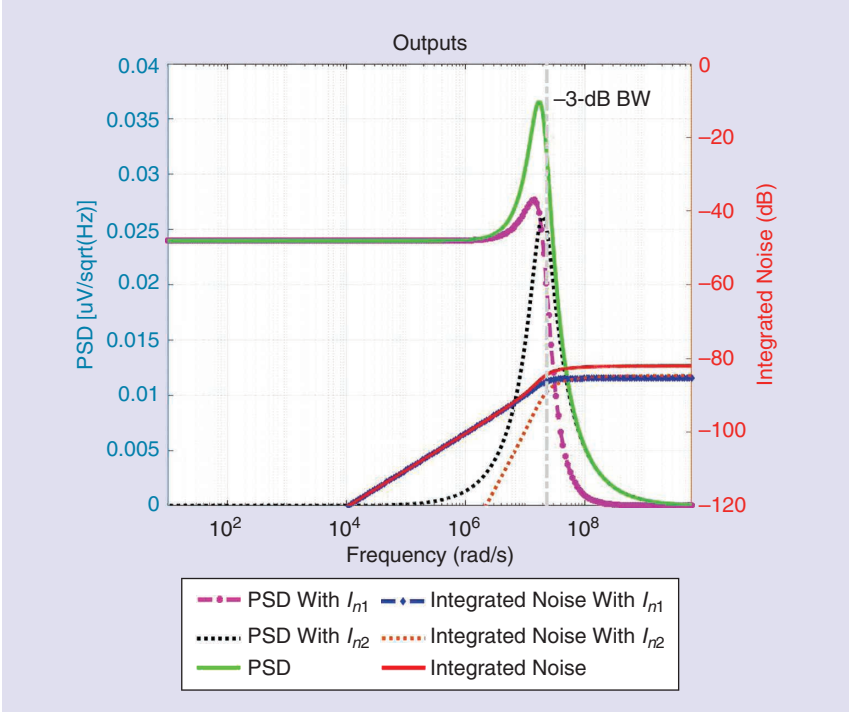

FIGURE 8: Noise PSD and integrated noise, I_{n1} and I_{n2}. BW: bandwidth.

For this notch filter, the –3-dB frequency can be defined as the signal bandwidth. From (7) and (8), the noise from R_1 and R_2 directly refers to the input, while the noise of R_3 and R_4 is high-pass filtered by C_B and R_4. The noise power spectrum density (PSD) and integrated noise plots are shown in Figure 8. At low frequency, R_1 and R_2 noise dominates. When going to higher frequencies, the noise of R_3 and R_4 comes into the picture. The overall integration noise at –3-dB frequency is around –84 dB.

References

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